November 2002

National Semiconductor

ADC12281
12-Bit, 20 MSPS Single-Ended Input, Pipelined A/D Converter

General Description

The ADC12281 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 20 megasamples per second (MSPS). It utilizes a pipeline architecture to minimize die size and power dissipation. Self-calibration and error correction maintain accuracy and performance over temperature.

The ADC12281 operates on a 5V power supply and can digitize single-ended analog input signals in the range of 0V to 2V. A single convert clock controls the conversion operation and all digital I/O is TTL compatible.

The ADC12881 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the single-ended analog input and an internal amplifier buffers the reference voltage input.

The Power Down feature reduces power consumption to 20 mW, typical.

The ADC12281 is available in the 32-lead TQFP package and is designed to operate over the industrial temperature range of −40˚C to +85˚C.

Features

- Single 5V power supply
- Single-ended analog input
- Internal sample-and-hold
- Internal reference buffer amplifier
- Low offset and gain errors

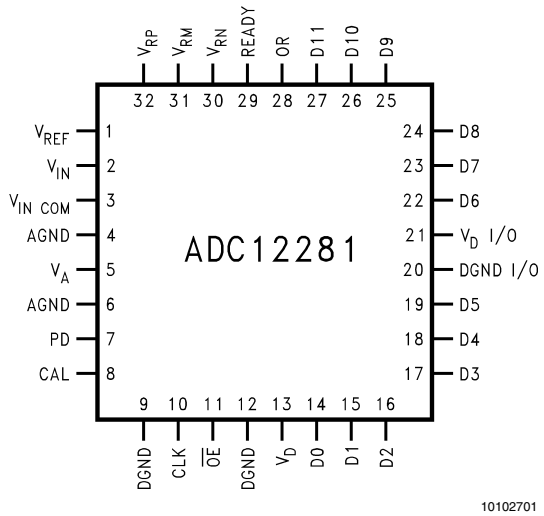
Key Specifications

■ Resolution	12 bits
■ Conversion rate	up to 20 MSPS
■ DNL	0.35 LSB (typ)
■ SNR	65.5 dB (typ)
■ ENOB	10.5 bits (typ)
■ Analog input range	2 V_{PP} (min)
■ Supply voltage	+5V ±5%
■ Power consumption, 20 MHz	443 mW (typ)

Applications

- Digital signal processing front end
- Digital television
- Radar
- High speed data links
- Waveform digitizers
- Quadrature demodulation

Connection Diagram



32-Lead TQFP Package
Order Number ADC12281CIVT
See NS Package Number VBE32A

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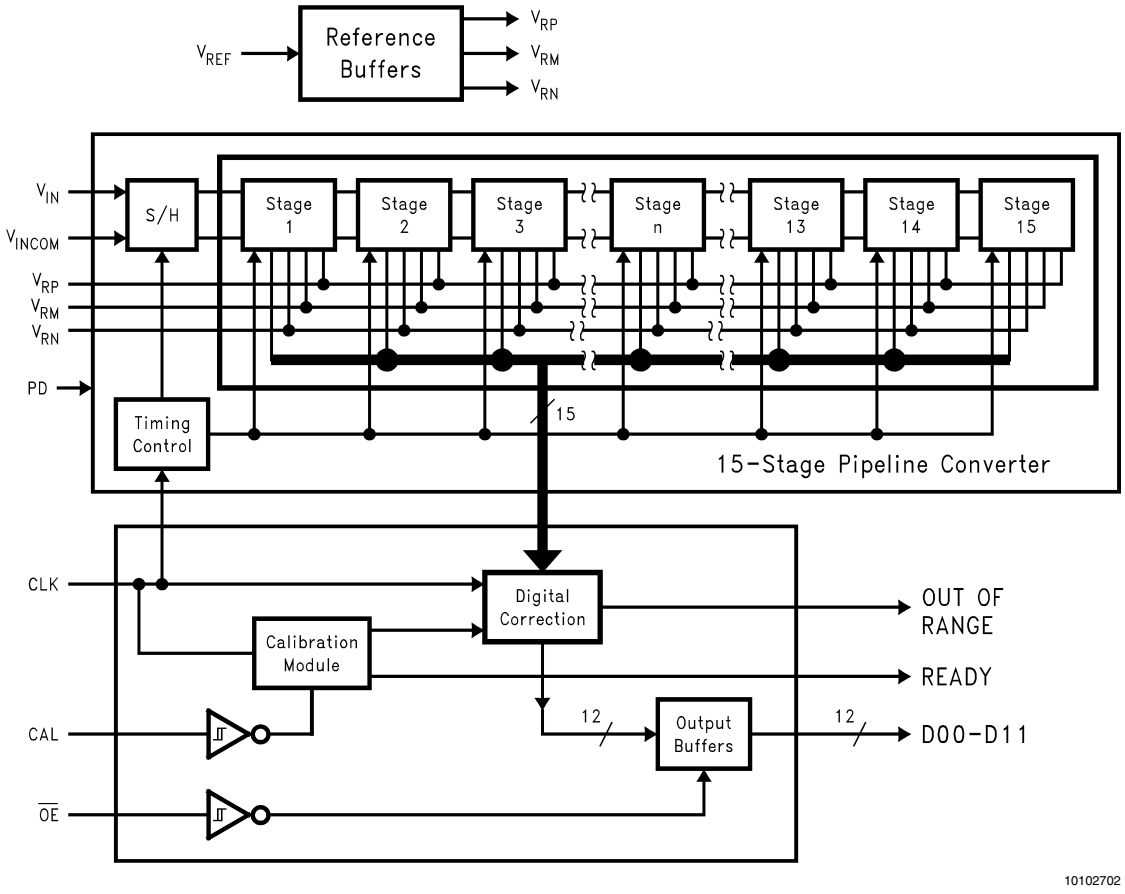
Ordering Information

Industrial (−40˚C ≤ T_A ≤ +85˚C)	Package
ADC12281CIVT	32-Pin TQFP

Simplified Block Diagram



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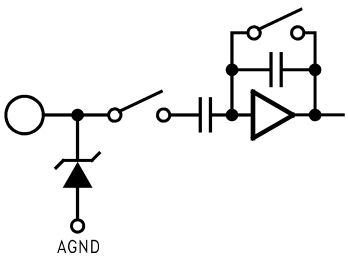
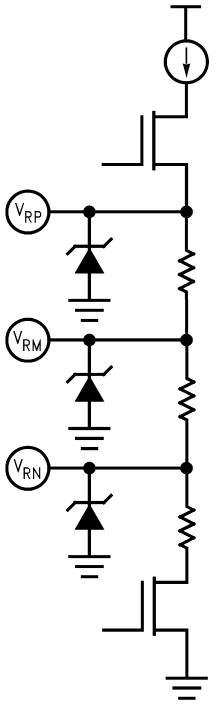
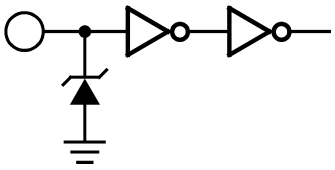
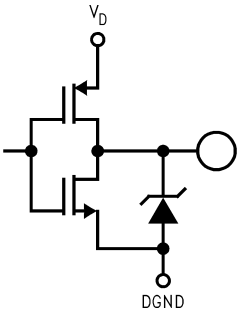
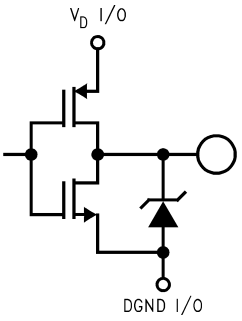
Pin Descriptions and Equivalent Circuits

Pin	Symbol	Equivalent Circuit	Description
2	V_{IN}		Single-ended analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0V to 2.0V will be converted. See Section 1.2.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8V to 2.2V and bypassed to a low-noise ground with a monolithic ceramic capacitor, nominally 0.01 µF. See Section 1.1.

Pin Descriptions and Equivalent Circuits (Continued)

Pin	Symbol	Equivalent Circuit	Description
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
30	V_{RN}		Negative reference bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
10	CLOCK		Sample clock input, TTL compatible. Amplitude should not exceed 3 V_{P-P}.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See Section 2.2.
7	PD		Power-down, active High, ignored during calibration cycle. See paragraph 2.4.
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in TRI-STATE® (high-impedance) mode.
28	OR		Over-range indicator. This pin is at a logic High, for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin will be at a logic Low during a calibration cycle and while the device is in the power down mode.
14–19, 22–27	D0–D11		Digital output word, CMOS compatible. D0 (pin 19) is LSB, D11 (pin 36) is MSB. Load with no more than 25 pF.

Pin Descriptions and Equivalent Circuits (Continued)

Pin	Symbol	Equivalent Circuit	Description
3	$V_{IN\ COM}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See Section 1.2.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5 µF to 10 µF capacitor and a 0.1 µF chip capacitor.
4, 6	AGND		The ground return for the analog supply, AGND and DGND should be connected together close to the ADC12281 package. See Section 5.0.
13	V_D		Positive digital supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5 µF to 10 µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC12281 package. See Section 5.0.
21	V_D I/O		The digital output driver supply pins. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage. See Section 3.4.
20	DGND I/O		The ground return for the digital output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12281.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltages (V_A, V_D, V_D I/O)	6.5V
$\|V_A - V_D\|$	≤100 mV
V_D I/O–V_A, V_D I/O–V_D	≤300 mV
Voltage on Any Input or Output Pin	−0.3V to V_A +0.3V
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature, Infrared, (10 sec.) (Note 6)	300˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage (V_A, V_D)	+4.75V to +5.25V
Output Driver Supply Voltage (V_D I/O)	+2.7V to V_D
V_{REF} Input	1.8V to 2.2V
CLOCK, CAL, PD, $\overline{OE}$	−0.05V to V_D +0.05V
Ground Difference |AGND–DGND|	≤100 mV

Converter Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 20 MHz, 3 V_{P-P} at 50% duty cycle, C_L = 25 pF/pin. After Auto-Cal. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C (Notes 7, 8, 9).

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12**	Bits (min)
INL	Integral Non-Linearity		±1.0	**±2.5**	LSB (max)
DNL	Differential Non-Linearity		±0.35	**±0.9**	LSB (max)
	Full-Scale Error		+3	**±10**	LSB (max)
	Zero Error		+7	**±17**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
BW	Full Power Bandwidth		100		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 4.43 MHz, V_{IN} = 2.0 V_{P-P}	65.5	**62.5**	dB (min)
SINAD	Signal-to-Noise and Distortion	f_{IN} = 4.43 MHz, V_{IN} = 2.0 V_{P-P}	65	**62**	dB (min)
ENOB	Effective Number of Bits	f_{IN} = 4.43 MHz, V_{IN} = 2.0 V_{P-P}	10.5	**10**	Bits (min)
THD	Total Harmonic Distortion	f_{IN} = 4.43 MHz, V_{IN} = 2.0 V_{P-P}	−76		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 4.43 MHz, V_{IN} = 2.0 V_{P-P}	75		dB
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Voltage Range			**V_{REF}**	V (max)
C_{IN}	V_{IN} Input Capacitance	(CLK LOW)	10		pF
		(CLK HIGH)	15		pF
V_{REF}	Reference Voltage (Note 14)		2.00	**1.8**	V (min)
				2.2	V (max)
	Reference Input Leakage Current		10		µA
	Reference Input Resistance		1		MΩ

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 20 MHz, 3 V_{P-P} at 50% duty cycle, C_L = 25 pF/pin. After Auto-Cal. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C (Notes 7, 8, 9).

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
CLOCK, CAL, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical "1" Input Voltage	V_D = 5.25V		**2.0**	V (min)

DC and Logic Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 20 MHz, 3 V_{P-P} at 50% duty cycle, C_L = 25 pF/pin. After Auto-Cal. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C (Notes 7, 8, 9).

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
V_{IL}	Logical "0" Input Voltage	V_D = 4.75V		**0.8**	V (max)
I_{IH}	Logical "1" Input Current	V_{IN} = 5.0V	10		µA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V	−10		µA
C_{IN}	Logic Input Capacitance		8		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −1 mA		**4**	V (min)
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 3V or 5V	100		nA
		V_{OUT} = 0V	−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_D I/O = 3V, V_{OUT} = 0V	−29		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_D I/O = 3V, V_{OUT} = V_D	28		mA
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = DGND (active)	85	**100**	mA (max)
		PD = V_D I/O (power-down mode)	3.5		mA
I_D	Digital Supply Current	PD = DGND (active)	3.6	**6**	mA (max)
		PD = V_D I/O (power-down mode)	1		mA
	Total Power Consumption	PD = DGND (active)	443	**530**	mW (max)
		PD = V_D I/O (power-down mode)	20		typ

AC Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 20 MHz, 3 V_{P-P} at 50% duty cycle, C_L = 25 pF/pin. After Auto-Cal. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C (Notes 7, 8, 9).

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
f_{CLK}	Conversion Clock (CLOCK) Frequency		0.5		MHz (min)
				20	MHz (max)
t_{CONV}	Conversion Latency			**10**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_D I/O = 3V	7		ns (max)
		V_D I/O = 5V	5	**17**	
I_{OZ}	Data Outputs into TRI-STATE Mode		16		ns
t_{OE}	Data Outputs Active after TRI-STATE		10		ns
t_{WCAL}	Calibration Request Pulse Width		3		T_{CLK}
t_{RDYC}	Ready Low after CAL Request		3		T_{CLK}
t_{CAL}	Calibration Cycle		4000		T_{CLK}
t_{WPD}	Power-Down Pulse Width		3		T_{CLK}
t_{RDYPD}	Ready Low after PD Request		3		T_{CLK}
t_{PD}	Power-Down Mode Exit Cycle		4000		T_{CLK}

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = DGND I/O = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A, V_D or V_D I/O), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

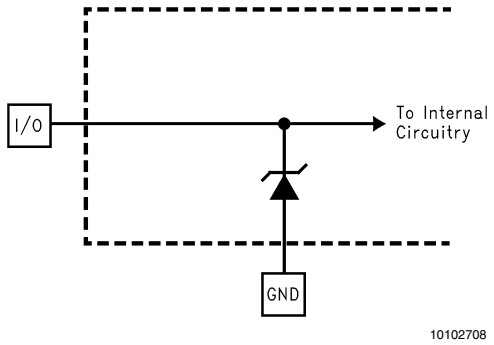
AC Electrical Characteristics (Continued)

Note 4: The absolute maximum junction temperature (T_{JMAX}) for this device is 150˚C. The maximum allowable power dissipation is dictated by T_{JMAX}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_D MAX = (T_{JMAX} − T_A) /θ_{JA}. In the 32-pin TQFP, θ_{JA} is 79˚C/W, so P_D MAX = 1,582 mW at 25˚C and 949 mW at the maximum operating ambient temperature of 75˚C. Note that the power dissipation of this device under normal operation will typically be about 125 mW (typical power dissipation + 20 mW TTL output loading). The values for maximum power dissipation listed above will be reached only when the ADC12281 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The inputs are protected as shown below. Input voltage magnitudes up to 5V above V_A or to 5V below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤ 4.85V to ensure accurate conversions.



ESD Protection Scheme for Analog Input and Digital Output Pins

Note 8: To guarantee accuracy, it is required that $|V_A - V_D| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.

Note 9: With the test condition for V_{REF} = +2.0V, the 12-bit LSB is 488 µV.

Note 10: Typical figures are at $T_A = T_J$ = 25˚C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Integral Non-Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero.

Note 13: Timing specifications are tested at the TTL logic levels, V_{IL} −0.4V for a falling edge and V_{IH} = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 14: Optimum SNR performance will be obtained by keeping the reference input in the 1.8V to 2.2V range. The LM4041CIM3-ADJ (SOT-23 package), the LM4041CIZ-ADJ (TO-92 package), or the LM4041CIM-ADJ (SO-8 package) bandgap voltage reference is recommended for this application.

Transfer Characteristics

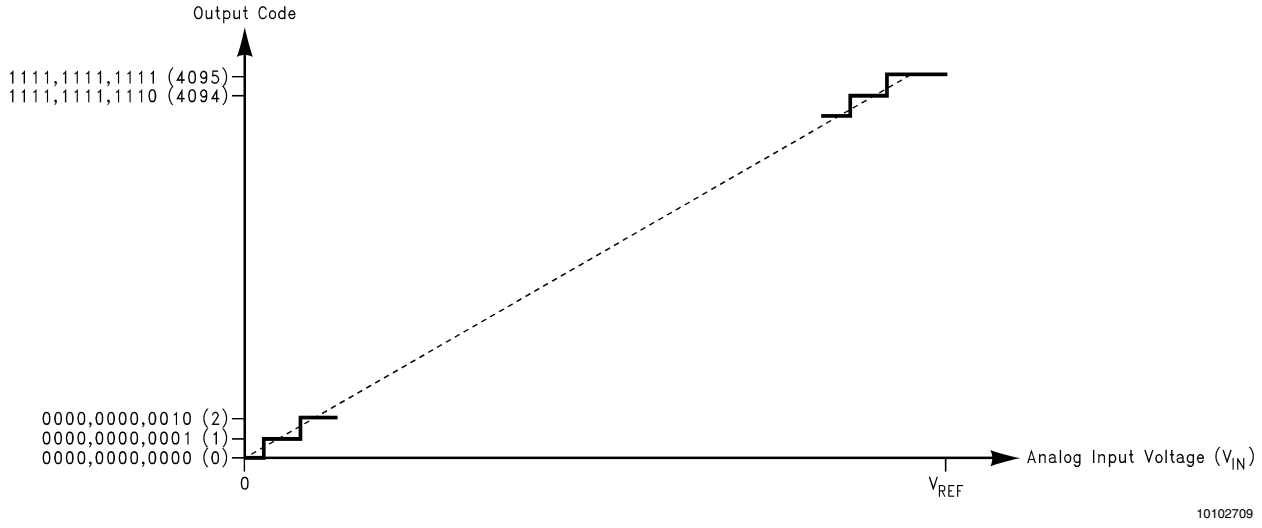


FIGURE 1. Transfer Characteristics

Transfer Characteristics (Continued)

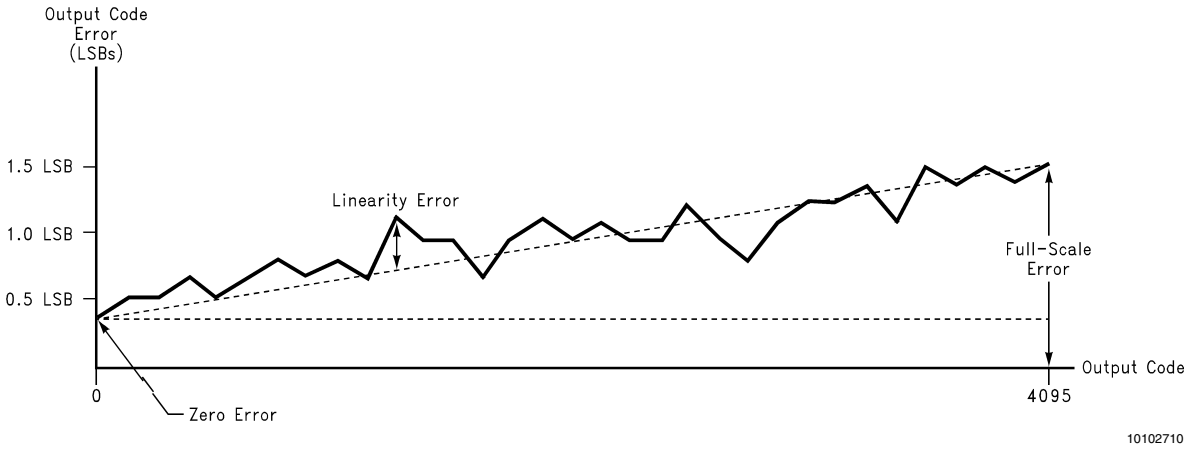
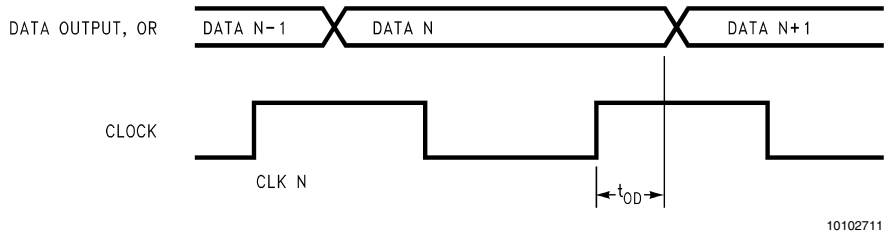
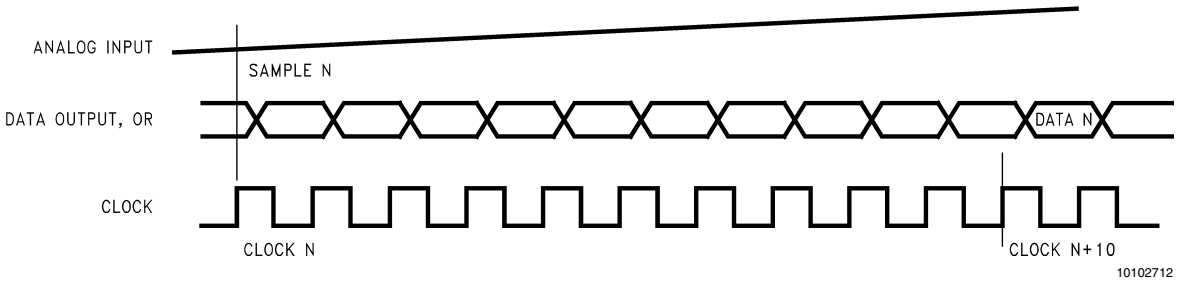


FIGURE 2. Errors Reduced after Auto-Cal Cycle

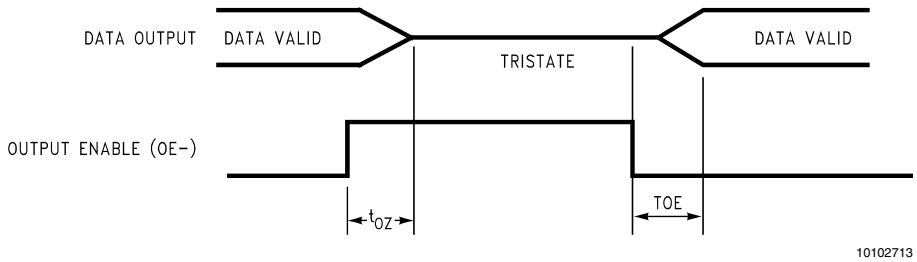
Timing Diagrams



Data Output Timing



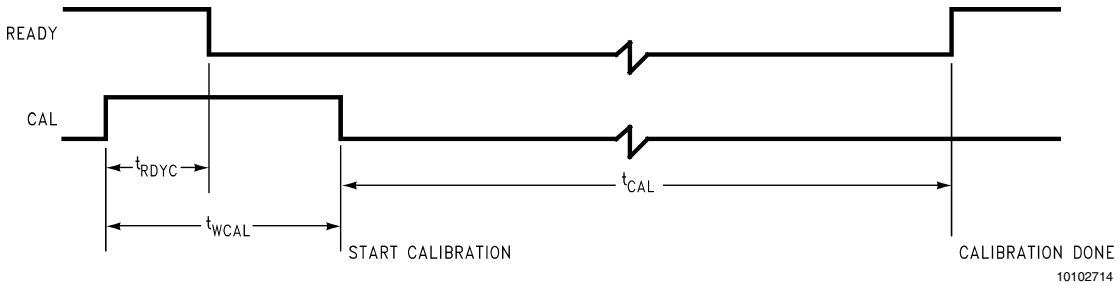
Data Output Latency



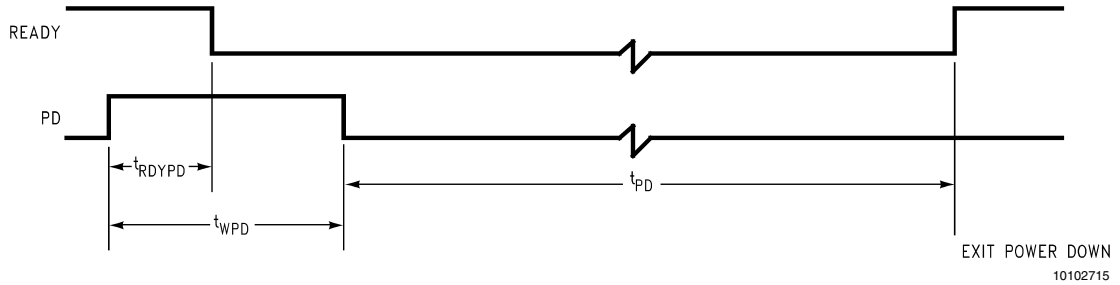
Data Output Enable

FIGURE 3. Data Output Timing

Timing Diagrams (Continued)



Calibration Request Cycle

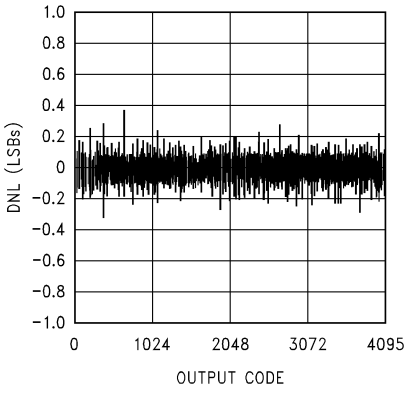


Power Down Request Cycle

FIGURE 4. Reset and Calibration Timing

Typical Performance Characteristics (V_A = V_D = V_D I/O = 5V, f_{CLK} = 20 MHz, unless otherwise stated)

DNL



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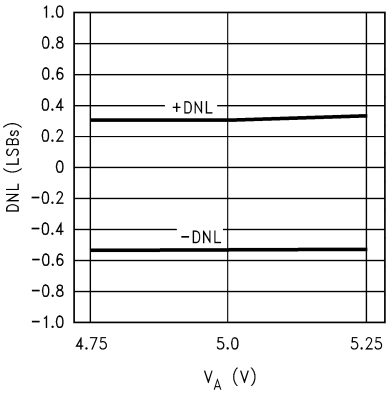
DNL vs V_A



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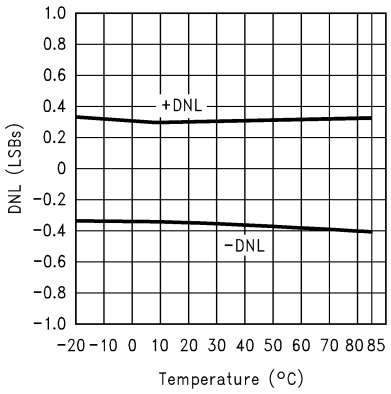
DNL vs Temperature



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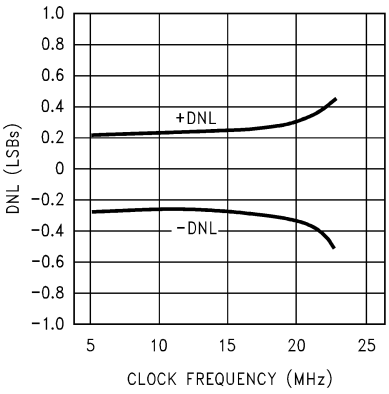
DNL vs f_{CLK}



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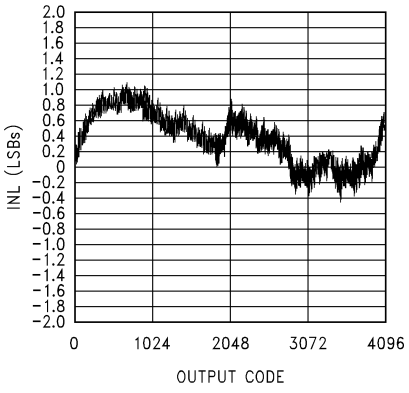
INL



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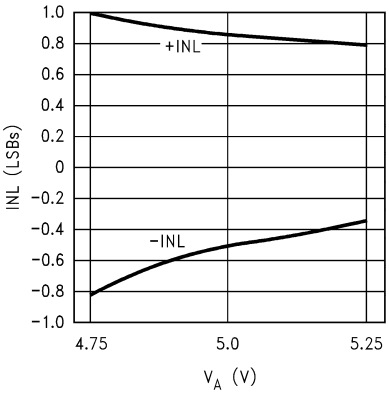
INL vs V_A



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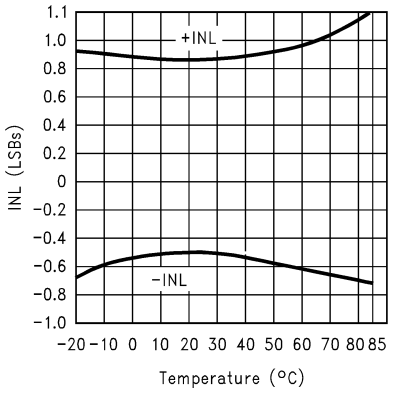
Typical Performance Characteristics (V_A = V_D = V_D I/O = 5V, f_{CLK} = 20 MHz, unless otherwise stated) (Continued)

INL vs Temperature



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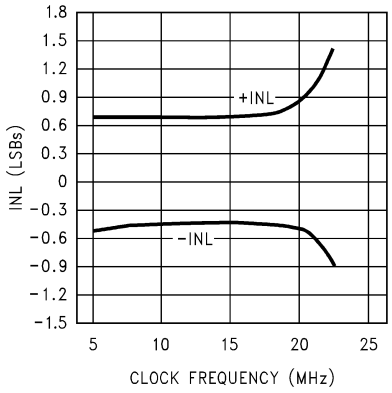
INL vs f_{CLK}



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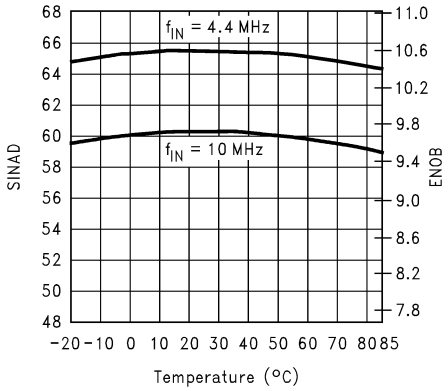
SINAD and ENOB vs Temperature



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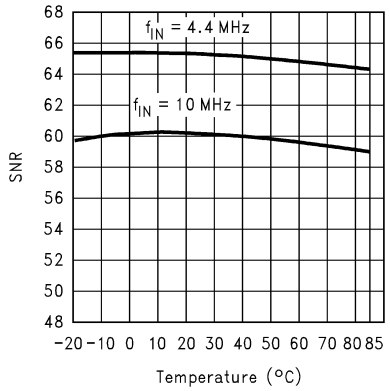
SNR vs Temperature



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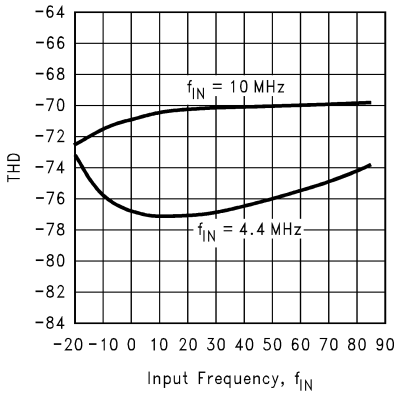
THD vs Temperature



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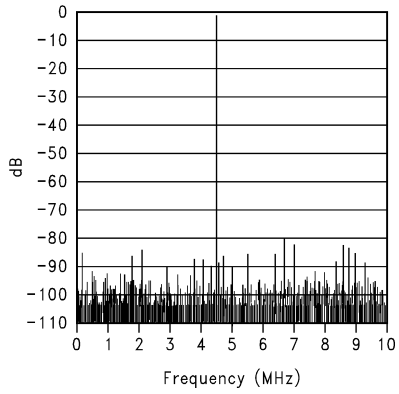
Spectral Response @ 20 MSPS



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Specification Definitions

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

APERTURE DELAY See Sampling Delay.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is high to the total time for one clock cycle.

CONVERSION LATENCY: See PIPELINE DELAY.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76)/6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL SCALE ERROR is the difference between the input voltage (V_{IN+}–V_{IN-}) just causing a transition to positive full scale and V_{REF} –1.5 LSB, where V_{REF} is ($V_{REF+\ IN}$) – ($V_{REF-\ IN}$).

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. INL is commonly measured at rated clock frequency with a ramp input.

OFFSET ERROR is the difference between the ideal LSB transition to the actual transition point. The LSB transition should occur when $V_{IN+} = V_{IN-}$.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and the availability of that same conversion result at the output. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay plus the Output Delay.

SAMPLING (APERTURE) DELAY is the time after the edge of the clock to when the input signal is acquired or held for conversion.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first six harmonic components to the rms value of the input signal.

ZERO SCALE OFFSET ERROR is the difference between the ideal input voltage (½ LSB) and the actual input voltage that just causes a transition from an output code of zero to an output code of one.

ZERO ERROR See Zero Scale Offset Error.

Functional Description

The ADC12881 is a monolithic CMOS analog-to-analog converter capable of converting single-ended analog input signals into 12-bit digital words at 20 megasamples per second (MSPS). This device utilizes a proprietary pipeline architecture and algorithm to minimize die size and power dissipation. The ADC12281 uses self-calibration and digital error correction to maintain accuracy and performance over temperature and a single-ended to differential conversion circuit to ease input interfacing while achieving differential input performance.

The ADC12281 has an input signal sample-and-hold amplifier and internal reference buffer. The analog input and the reference voltage are converted to differential signals for internal use. Using differential signals in the analog conversion core reduces crosstalk and noise pickup from the digital section and power supply.

The pipeline conversion core has 15 sequential signal processing stages. Each stage receives an analog signal from the previous stage (called “residue”) and produces a 1-bit digital output that is sent to the digital correction module. At each stage the analog signal received from the previous stage is compared to an internally-generated reference level. It is then amplified by a factor of 2, and, depending on the output of the comparator, the internal reference signal may be subtracted from the amplifier output. This produces the residue that is passed to the next stage.

The calibration module is activated at power-on or by user request. During calibration the conversion core is put into a special mode of operation in order to determine inherent errors in the analog conversion blocks such as op amp offsets, comparator offsets, capacitor mismatches, etc. The calibration procedure determines coefficients for each digital output bit from the conversion core and stores these coefficients in on-chip RAM. The digital correction module uses the coefficients in RAM to convert the raw data bits from the conversion core into the 12-bit digital output code.

Applications Information

1.0 ANALOG INPUTS

The analog inputs of the ADC12881 are the reference input (V_{REF}) and the signal input (V_{IN}).

Reference Input

The V_{REF} input must be driven from an accurate, stable reference voltage source between 1.8V and 2.2V and bypassed to a clean, low-noise ground with a monolithic ceramic capacitor (nominally 0.01 µF).

Analog Signal Input

This analog input is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 10 pF when the clock is low, and 15 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than is a fixed capacitance, choose an amplifier that can drive this type of load. The CLC409 has been found to be a good device to drive the ADC12281. Do not drive the input beyond the supply rails.

The V_{IN} input must be driven with a low impedance signal source that does not add any distortion to the input signal. The ground reference for the V_{IN} input is the $V_{IN\ COM}$ pin. The $V_{IN\ COM}$ pin should be connected to a clean point in the

Applications Information (Continued)

analog ground plane. The ground return for the reference voltage should enter the ground plane at the same point as does the $V_{IN\ COM}$ pin.

To simplify the interface, the ADC12281 has an internal single-ended to differential buffer. This permits performance you would expect to see with a differential input while driving the input with a single-ended signal.

To achieve maximum performance, you should be careful to maintain short input and ground runs in lines carrying signal current. The signal ground line, $V_{IN\ COM}$ and the reference ground should all enter the analog ground plane at the same point, as indicated in *Figure 5*.

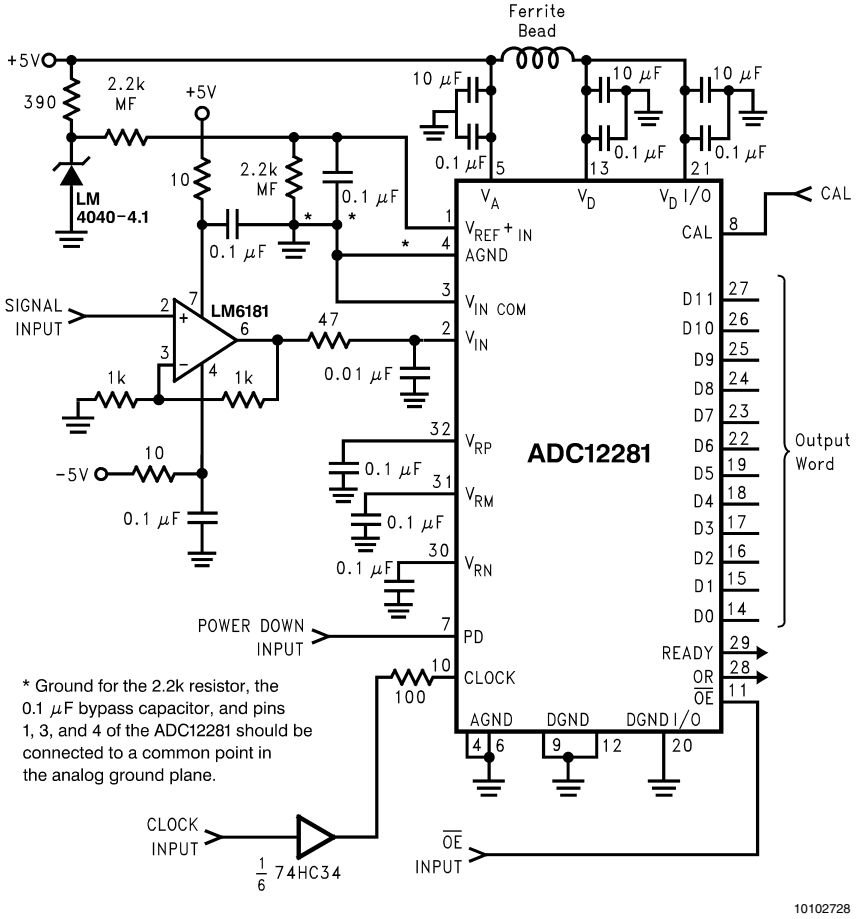


FIGURE 5. Suggested Application Circuit

2.0 DIGITAL INPUTS

The ADC12281 has four digital inputs. They are CLOCK, CAL, $\overline{OE}$ and PD.

The **CLOCK** input should be driven with a stable, low phase jitter TTL level clock signal in the range of 0.5 MHz to 20 MHz. The clock high level should be limited to 3 V_{P-P} for maximum SNR performance and to meet data sheet performance specifications. The trace carrying the clock signal should be as short as possible. This trace should not cross any other signal line, analog or digital, not even at 90˚.

The level sensitive **CAL** input must be pulsed high for at least three clock cycles to begin ADC calibration. For best performance, calibration should be performed about ten seconds after power up, after resetting the ADC and whenever the temperature has changed by more than 25˚C since the last calibration cycle. Calibration should be performed at the same clock frequency that will be used for conversions.

Calibration takes 4000 clock cycles to be performed. **Irrelevant data may appear at the data outputs during CAL.**

The $\overline{OE}$ pin is used to READ the conversion. When the $\overline{OE}$ pin is low, the output buffers return to the active state. When the $\overline{OE}$ input is high, the output buffers are in the high impedance state.

The PD pin, when high, holds the ADC12281 in a power-down mode where power consumption is typically less than 15 mW to conserve power when the converter is not being used. The ADC12281 will begin normal operation with t_{PD} after this pin is brought low, provided a valid CLOCK input is present. The data in the pipeline is corrupted while in the power-down mode. The ADC12281 does not have to be re-calibrated after a power-down cycle unless the power supply voltage or ambient temperature has changed.

Applications Information (Continued)

3.0 OUTPUTS

The ADC12281 has three analog outputs: reference output voltages V_{RN}, V_{RM}, and V_{RP}. There are 14 digital outputs: 12 Data Output pins, OR (Over-range) and Ready.

The reference output voltages are made available only for the purpose of bypassing with capacitors to a clean analog ground. The recommended bypass capacitors are 0.1 µF ceramic chip capacitors.

DO NOT LOAD reference bypass pins 30, 31 or 32.

The OR output goes low to indicate the presence of valid data at the output data lines. The signal will go high when the analog input is above the V_{REF} input or below GND.

The READY output, when at a logic high, indicates that the ADC12281 is ready to convert. This output is at a logic low during a calibration cycle and when the ADC12281 is in the power down mode.

The Data Outputs are TTL/CMOS compatible. The output data format is 12 bits straight binary. The V_D I/O provides power for the output driver and may be operated from a supply in the range of 3.0V to the V_D supply (nominal 5V). This can simplify interfacing to 3.0V devices and systems.

Powering the V_D I/O from 3V will also reduce power consumption and noise generation due to output switching. **DO NOT operate the V_D I/O at a voltage higher than V_D or V_A!**

Also helpful in minimizing noise due to output switching is to minimize the currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry. Only one buffer should be connected to each output. Additionally, inserting series resistors of 47Ω to 56Ω right at the digital outputs, close to the ADC pins, will isolate the outputs from other circuitry and limit output currents.

4.0 POWER SUPPLY CONSIDERATIONS

Each power pin should be bypassed with a parallel combination of a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. The chip capacitors should be within 1/2 centimeter of the power pins. Leadless chip capacitors are preferred because they provide low lead inductance.

The converter's digital logic supply (V_D) should be well isolated from the supply that is used for other digital circuitry on the board. A common power supply should be used for both V_A (analog supply) and V_D (digital supply), and each of these supply pins should be separately bypassed with a 0.1 µF ceramic capacitor and a low ESR 10 µF electrolytic capacitor. A ferrite bead or inductor should be used between V_A and V_D to prevent noise coupling from the digital supply into the analog circuit.

V_D I/O is the power pin for the output buffers. This pin may be supplied with a potential between 2.7V and V_D. This makes it easy to interface the ADC12281 with 3V or 5V logic families.

The voltage at V_D I/O should never exceed the voltage at either V_A or V_D. All power supplies connected to the device should be applied simultaneously.

As is the case with all high speed converters, the ADC12281 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be minimized.

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC12281 are required to achieve specified performance. The analog and digital grounds may be in the same layer, but should be separated from each other and should never overlap each other. Separation between the analog and digital ground planes should be at least 1/8 inch, were possible.

The ground return for the digital supply (DGND I/O) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DGND I/O pin should NOT be connected to system ground in close proximity to any of the ADC12281's ground pins.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry separated from the digital circuitry and from the digital ground plane.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

Applications Information (Continued)

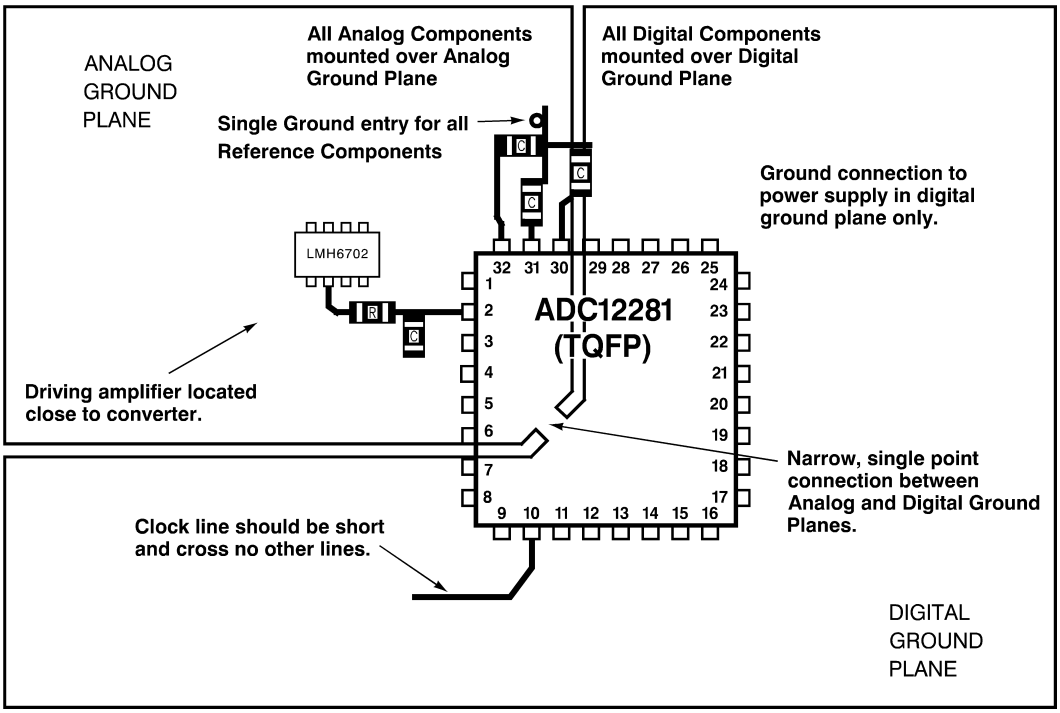


FIGURE 6. Example of a Suitable Layout

6.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or more than a volt below ground. A resistor of about 50Ω to 100Ω in series with the offending digital input will eliminate the problem.

Do not allow input voltages to exceed the supply voltage during power up.

Be careful not to overdrive the inputs of the ADC12281 with a device that is powered from supplies outside the range of the ADC12281 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_D I/O and DGND I/O. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem. The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12281, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω.

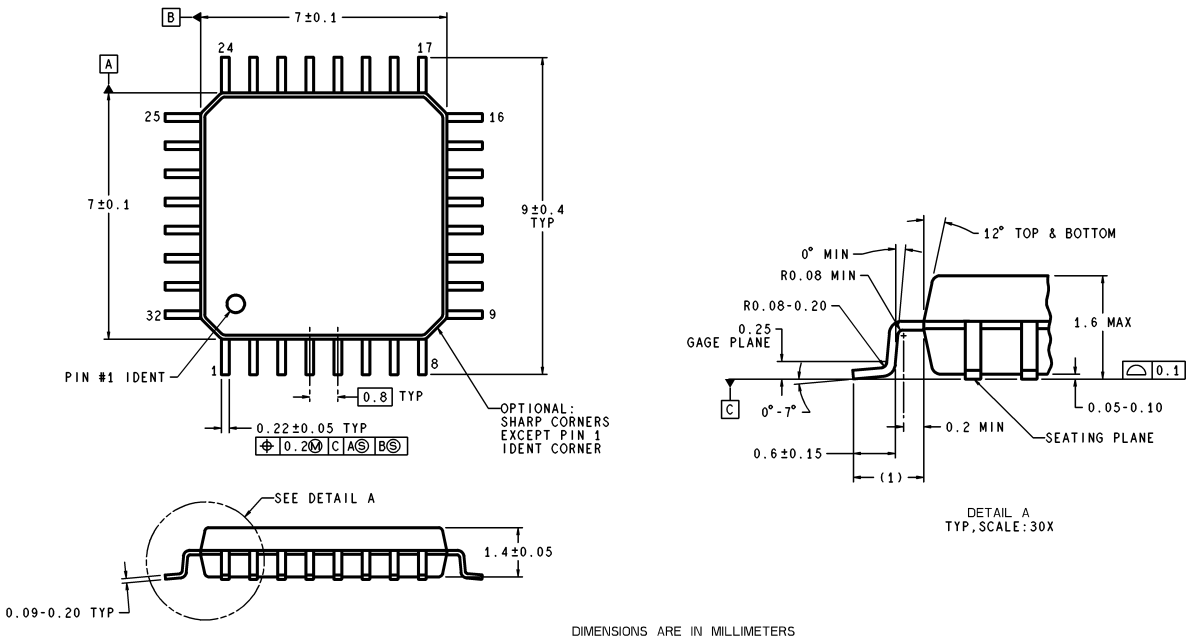
Using an inadequate amplifier to drive the analog input. As explained in Section 1.2, the capacitance seen at the input alternates between 12 pF and 28 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. The CLC409 has been found to be a good amplifier to drive the ADC12281. A small series resistor at the amplifier output, followed by a capacitor to ground (as shown in *Figure 5*), will improve performance.

Operating with the reference pins outside of the specified range. As mentioned in Section 1.1, V_{REF} should be in the range of $1.8V \leq V_{REF} \leq 2.2V$. Operating outside of these limits could lead to output distortion.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

Physical Dimensions inches (millimeters)
unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

VBE32A (Rev E)

32-Lead TQFP Package
Order Number ADC12281CIVT
NS Package Number VBE32A

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